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Electromagnetic interference reduction by dynamic impedance balancing applied to biosensors

João Francisco Ribeiro Negrão*, Guilherme Augusto Limeira Araujo, Carlos Tavares da Costa Júnior, Daniel Cardoso de Souza

Abstract ***Introduction:*** *Electromagnetic interference caused by electric power lines adversely affects the signals of electronic instruments, especially those with low amplitude levels. This type of interference is known as common-mode interference. There are many methods and architectures used to minimize the influence of this kind of interference on electronic instruments, the most common of which is the use of band-reject filters. This paper presents the analysis, development, prototype and test of a new reconfigurable filter architecture for biomedical instruments, aiming to reduce the common-mode interference and preserve the useful signal components in the same frequency range as that of the noise, using the technique of dynamic impedance balancing.* ***Methods:*** *The circuit blocks were mathematically modeled and the overall closed-loop transfer function was derived. Then the project was described and simulated in the VHDL_AMS language and also in an electronics simulation software, using discrete component blocks, with and without feedback. After theoretical analysis and simulation results, a prototype circuit was built and tested using as input a signal obtained from ECG electrodes.* ***Results:*** *The results from the experimental circuit matched those from simulation: a 97.6% noise reduction was obtained in simulations using a sinusoidal signal, and an 86.66% reduction was achieved using ECG electrodes in experimental tests. In both cases, the useful signal was preserved.* ***Conclusion:*** *The method and its architecture can be applied to attenuate interferences which occur in the same frequency band as that of the useful signal components, while preserving these signals.*

Keywords *Biomedical instruments, Electromagnetic interference, Common-Mode Rejection, Instrumentation amplifier, Dynamic impedance balancing.*

*e-mail: jfrn@ufpa.br
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Introduction

Electromagnetic Interference (EMI) is a deleterious phenomenon that affects the operation of electronic devices (Yamamoto *et al*., 2000), and one of the main factors that lead to a noise increase due to EMI is impedance unbalance. Impedance balancing is a technique to compensate for the impedance mismatch (unbalance) of the biopotential electrodes' inputs or amplifier inputs, in order to provide a high Common-Mode Rejection Ratio (CMRR) to the instrumentation system. If those impedances are unbalanced, the gain and the CMRR of the signal processing circuit will be strongly degraded. These deleterious effects can be reduced using both electronic and mechanical techniques, such as increasing the CMRR of the signal processing circuit (Degen and Jackel, 2008; Grimbergen *et al*., 1996; Spinelli *et al*., 2004, 2006), or shielding the data cables by an external metal mesh.

The loss of signal strength due to the unbalance in electrode wires or input terminals tends to increase as distance grows between the transducers or sensors and the input circuits. Some techniques, such as the Instrumentation Amplifier (IA) architecture (Dobrev and Daskalov 2009), can reduce the common-mode interference (V_{cm}) range about 200 times, when applied to an electrocardiogram signal (Berbari, 2000) (Figure 1). Some authors like Degen (Degen and Jackel, 2008) proposed to reduce the unbalance, caused by sensor disconnection of the patient's skin, by monitoring a reference voltage generated by a "driven-right-leg circuit (DRL)", while Spinelli (Spinelli *et al*., 2006), also working in the same unbalance mentioned by Degen, proposed a circuit using an instrumentation amplifier and a low pass filter (LPF) and shielded cables.

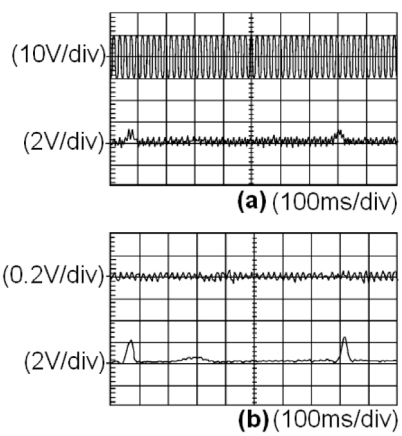

Figure 1. ECG signal influenced by V_{cm} noise, (a) without balancing and (b) with balancing (Dobrev and Daskalov, 2009). In Figures 1a, b, the upper graph represents the V_{cm} noise (electric power 50 Hz sine wave), and the lower graph represents the differential signal before and after balancing.

This work proposes a new control method, which uses dynamic impedance balancing (real-time) to reduce the effect of V_{cm} in electronic circuits, mainly generated by the electric power line (60 Hz). A new architecture is proposed using discrete components which reduces the V_{cm} interference while preserving the differential-mode signal (V_d). Finally, a prototype is built and tested to evaluate the applicability of this architecture. This circuit presents reconfigurable characteristics and could be easily used in any noise range by reprogramming the microprocessor which controls the band pass filters (BPF). The prototype circuit design is based on the reconfigurability concept (Negrão *et al*., 2006). A model described in VHDL-AMS (Mentor Graphics, 2006) allows us to validate the basic principles of operation, and the software "Isis Proteus Schematic Capture" (Labcenter Electronics, 1989-2009) is used for the design of a test version with discrete components. The experimental results validate those obtained in simulation.

Theoretical Foundation

The architecture proposed in this paper aims to attenuate V_{cm} by reducing the amount of impedance unbalance. However, when compared to other methods (Degen and Jackel 2008; Grimbergen *et al*., 1996; Spinelli *et al*., 2004, 2006), the approach presented here has the advantage of attenuating only V_{cm}, with small impact on the useful signal components (V_d), even if they are in the same frequency range as the noise.

The unbalance of the electrodes' input impedances is dynamically compensated for by a counter circuit in a feedback system (the RECONFIGURABLE CIRCUIT), which controls a bank of impedances as shown in Figure 2. The structure and operation of the circuit are described below.

Where:

V_{cm} = common-mode interference (noise) signal;

$V_{d/2}$ = biopotential signal at each electrode;

V_+ and V_- = voltages at the IA input;

Z_1 and Z_2 = impedances of the input electrodes;

Z_{c1} and Z_{c2} = dynamically-adjustable impedances;

Z_{in} = IA input impedance;

RECONFIGURABLE CIRCUIT = circuit responsible for dynamically controlling the adjustable impedances;

V_0 = adjusted output signal.

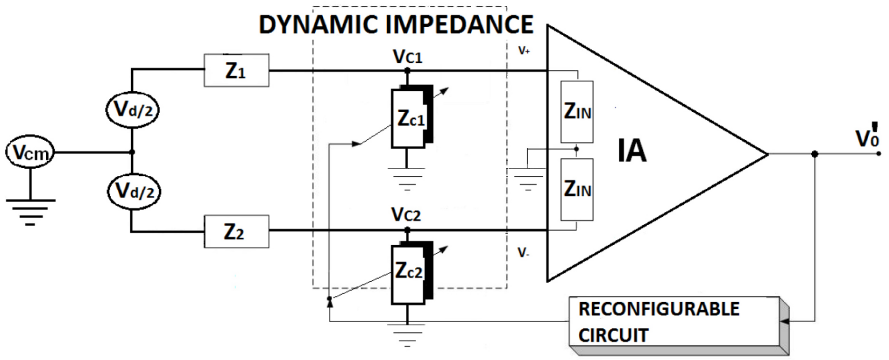

Figure 2. New architecture proposed, adapted from (Silva, 2003).

The impedance unbalance reduction is viable by means of a feedback loop (RECONFIGURABLE CIRCUIT) which, depending on the variation of the maximum amplitude of the output signal (V_0'), readjusts the values of the input impedances (Z_{C1} and Z_{C2}) to yield an output signal with minimal interference. These values are achieved when the impedance balancing condition of Equation 1 (Dobrev and Daskalov, 2009) is satisfied, meaning that the common-mode noise was canceled.

$$Z_{c1} + Z_1 = Z_{c2} + Z_2 \tag{1}$$

The general equation of a non-feedback amplifier is only governed by its internal components, and it is shown in Equation 2, where A_{cm} is the common-mode gain of the amplifier, and A_d is the differential-mode gain of the amplifier. Equation 3 defines the transfer function of our architecture (Figure 2), using the principle of feedback by reconfigurability (Negrão *et al*., 2006). Equation 3 is composed of three terms, but since our main analysis goal in this work is the noise component V_{cm}, and not V_d or the CMRR, only the second term of Equation 3 will be taken into consideration. This yields a revised V_0' (Equation 4), which is directly influenced by the balancing of the cable impedances (Z_1, Z_2, and Z_{C1}, Z_{C2}), the noise (V_{cm}) and the A_d at the IA inputs. The new V_0' in equation 4 will be used in the rest of this paper. Equation 5 is used to measure the level of unbalance determined by the new proposed architecture. This is the same method used to determine the level of unbalance in longitudinal telephone cables (Volpato and Magalhães, 2009). After appropriate values (Z_{C1} = 2.5 MΩ, Z_{C2} = 10 kΩ, $Z_1 = Z_2$ = 1.2 MΩ) are replaced in Equation 6, the worst-case unbalance value predicted for the architecture is BAL = –0.6674 dB.

$$V_0' = V_d \cdot A_d + V_{cm} \cdot A_{cm} \tag{2}$$

$$V_0' = \left\{ \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c1}\cdot Z_{in})}{\left[Z_1(Z_{c1}+Z_{in})+(Z_{c1}\cdot Z_{in})\right]} - \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c2}\cdot Z_{in})}{\left[Z_2(Z_{c2}+Z_{in})+(Z_{c2}\cdot Z_{in})\right]} \right\} \cdot \frac{V_d}{2} \cdot A_d + \left\{ \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c1}\cdot Z_{in})}{\left[Z_1(Z_{c1}+Z_{in})+(Z_{c1}\cdot Z_{in})\right]} - \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c2}\cdot Z_{in})}{\left[Z_2(Z_{c2}+Z_{in})+(Z_{c2}\cdot Z_{in})\right]} \right\} \cdot V_{cm} \cdot A_d + V_{cm} \cdot \frac{A_d}{CMRR} \tag{3}$$

$$V_0' = \left\{ \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c1}\cdot Z_{in})}{\left[Z_1(Z_{c1}+Z_{in})+(Z_{c1}\cdot Z_{in})\right]} - \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c2}\cdot Z_{in})}{\left[Z_2(Z_{c2}+Z_{in})+(Z_{c2}\cdot Z_{in})\right]} \right\} \cdot V_{cm} \cdot A_d \tag{4}$$

$$BAL = 20 \cdot \log \left| \frac{V_{C2} - V_{C1}}{V_{cm}} \right| \ (dB) \tag{5}$$

$$BAL = 20 \cdot \log \left| \frac{\frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c2}\cdot Z_{in})}{\left[Z_2(Z_{c2}+Z_{in})+(Z_{c2}\cdot Z_{in})\right]} - \frac{\left(V_{cm} + \frac{V_d}{2}\right)\cdot(Z_{c1}\cdot Z_{in})}{\left[Z_1(Z_{c1}+Z_{in})+(Z_{c1}\cdot Z_{in})\right]}}{V_{cm}} \right| \ (dB) \tag{6}$$

Where $V_d = V_{d/2} + V_{cm}$.

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Methods

Circuit modeling

The operation of the circuit is described by the algorithm shown in Figure 3.

The operational principle for the proposed circuit is based on signal compensation, comprising a common-mode component (V_{cm}) and a differential-mode component (V_d), which are modulated by the input impedances (Z_{VAR}) formed by a resistor bank. These resistors are dynamically connected to the circuit and they may add up to a maximum value of 2.55 MΩ. This is possible with the use of analog switches, each controlled by a four-bit counter. As the signal amplitude is low, it needs to be amplified, and that is done by the IA. A sample of the signal after filtering by the 2nd-order LPF (V_O) is sent to be analyzed later with an oscilloscope. Another sample of the signal, after being filtered by a 4th-order BPF (V_1) with 30 Hz bandwidth (which allows only the EMI components between 40 and 70 Hz to pass), passes through the A/D converter implemented in the PIC16F877 microcontroller (with an 8-bit data bus, 4 MHz clock, 2400 bps processing capacity, and a 19.53 mV resolution).

This is what distinguishes this prototype from those submitted in earlier works (Dobrev and Daskalov, 2002; Negrão *et al*., 2006; Spnelli *et al*., 2004): the analysis of noise (V_{cm}), separated from the useful signal (V_d).

After the signal is sampled and processed with 8 bits of definition, there are 255 discrete voltage values (decimal values), which means that each level in the ladder conversion is 19.53 mV, for a 5 V reference voltage. As the signal at the IA output (INA 122) (V_0' as observed in the algorithm of Figure 3) is at a dc offset level of 2.5 V, then this point is now used as a reference when analyzing the V_{cm} noise, after being separated from V_d by the BPF. A software written in the C++ programming language has been implemented in the PIC microcontroller, to diagnose whether the amplitude of V_{cm} is within a reference range between 2.48031 V ("01111111") and 2.51937 V ("10000001"), around the central point (or dc level) of 2.49 V ("10000000"). If this sample level remains within this range, then it is considered that the dynamic impedance circuit (Z_{var}) is minimally balanced, in which case a signal at ground level (zero volts), is sent to turn off the clock of the counter circuit (Ctrl_U/D), but if the noise level of the sample is beyond the amplitude reference range, then it is considered that the dynamic impedance circuit is unbalanced. In this case, a high level (5V) is sent to turn on the clock of the counter circuit (Ctrl_U/D), and another high level prompting positive increment of the counter (UP), increasing the equivalent impedance of the block (Z_{var}). As the sampling process happens every 1 millisecond, the system is dynamically fed back by the most recent sample and if this sample indicates that the V_{cm} amplitude still increased even outside the reference range (even after 3 clock cycles, or 3 ms), the system considers that the action of counting up is incorrect, and then a low level (zero volts) is sent to the loop counter for decrementing the dynamic impedance (DW), to find again a balance of Z_{var}. When balance is found, the clock counter circuit is switched off again and waits for instructions to turn the system on again in order to conserve battery power. However, it is observed that the electromagnetic noise amplitude changes constantly and the system stays on continuously.

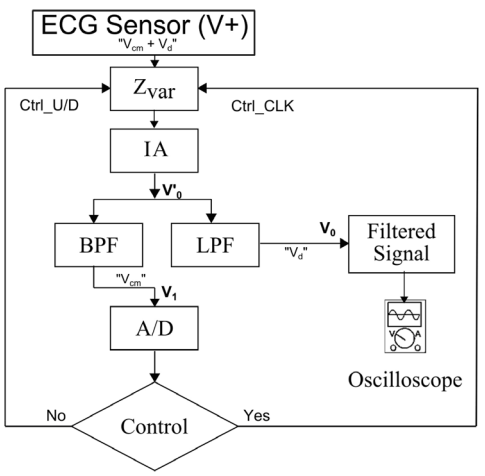

Figure 3. Circuit algorithm.

Variable impedance block

The variable impedance block consists of a group of resistances (Z_c), which is described by equation 7.

$$Z_{C_2} = R \cdot \sum_1^{NB} 2^{(NB-1)} \quad (7)$$

Where:

R is the first resistance value;

NB is the number of bits used in the A/D converter.

The circuit is completed with analog switches and counters, as detailed in Table 1.

Instrumentation amplifier block (IA)

Besides the implementation of an IA, a high-pass filter (HPF) was added to minimize the noise below 0.3 Hz (Equation 8), while the IA gain (G_{IA}) is given by equation 9.

$$|H(S)| = \frac{\omega \cdot C \cdot R}{\sqrt{1+(\omega \cdot C \cdot R)^2}} \quad (8)$$

$$G_{IA} = 5 + \frac{200K}{R_G} \quad (9)$$

Where:

R_G is the gain resistance, located inside the IA block (Figure 7 and Table 1);

ω is angular velocity.

The gain is kept at low levels in the IA ($G_{IA} \approx 14$ dB) to avoid saturating the filter blocks.

Low-pass and band-bass filters block

The filters design was based on the RAUCH architecture, in which the multiple feedback (MFB) topology is characterized by high gains and quality factor (Q), and its general transfer function is shown in Equation 10.

$$\frac{Z_{out}}{Z_{in}} = \frac{-1}{\left[\frac{R_3}{R_5} + \frac{R_1}{R_5} + \frac{R_1}{R_4} + \frac{R_1 \cdot R_3}{R_2 \cdot R_5} + \frac{R_1 \cdot R_3}{R_4 \cdot R_5}\right]} \quad (10)$$

From this standard block, after the appropriate resistance and capacitance values are replaced, other filters can be quantified: a 2nd-order LPF and its corresponding transfer function shown in equations (11, 12, 13 and 14), and a BPF composed of two cascaded 2nd-order blocks, each one described by equations (15, 16, 17 and 18), equivalent to a 4th-order filter. All the filter parameters have been calculated to yield a 3 dB attenuation. In the output of the BPF block, the signal intentionally received a higher gain as compared to other blocks.

$$|H(S)|_{LPF} = \frac{a_0}{b_1 S^2 + a_1 S + \omega_0^2} \quad (11)$$

$$a_0 = -\frac{R_2}{R_1} \quad (12)$$

$$a_1 = \omega_0 \cdot C_1 \cdot \left(R_2 + R_3 + \frac{R_2 \cdot R_3}{R_1}\right) \quad (13)$$

$$b_1 = \omega_0^2 \cdot C_1 \cdot C_2 \cdot R_2 \cdot R_3 \quad (14)$$

$$|H(S)|_{BPF\_2^o} = \frac{a_1 \cdot S}{b_1 S^2 + b_2 S + \omega_0^2} \quad (15)$$

$$a_1 = -\left(\frac{R_2 \cdot R_3}{R_1 + R_3}\right) \cdot C \cdot \omega_0 \quad (16)$$

$$b_1 = \left(\frac{R_3 \cdot R_2 \cdot R_3}{R_1 + R_3}\right) \cdot C^2 \cdot \omega_0^2 \quad (17)$$

$$b_2 = \left(\frac{2 \cdot R_1 \cdot R_3}{R_1 + R_3}\right) \cdot C \cdot \omega_0 \quad (18)$$

Where:

ω_0 is the fundamental angular velocity.

Control block

The control block is formed by the PIC microcontroller (Table 1, Figure 7) and a DC level shifter circuit to keep a 2.5 V reference. A better description of the control block is given above, on the "Circuit modeling" section.

Transfer functions

As all the main sub-circuits have been mathematically presented, the overall closed-loop transfer function (Equation 24) is shown in Figure 4.

The transfer function (Equation 24) could be used to analyze how all the sub-circuits in the system affect the output signal. For instance, taking as reference the control signal (Sc(s)) which represents the processing and control system block, if this signal is not properly

Table 1. List of components and description.

	Component	Quant.	Specification	Description
VARIMP	Resistor (Ω)	12	10k, 20k, 40k, 80k, 160k, 320k, 640k, 1280k, 2.55M, 2x100k.	Carbon resistor.
	Analog Switch	8	HEF4016 (Philips Semiconductors)	Analog switch.
	Counter	2	CD4029 (Philips Semiconductors)	Digital counter.
IA	IA	1	INA122 (Burn-Brown)	Instrumentation amplifier.
	R_G (Ω) (Pins 1 and 8 of the INA122)	1	200K	Variable resistor (trimpot).
FIL	Filter LPF (2nd order)	1	OP 07 (Texas Instruments)	Active Filter - 4 kHz.
	Filter BPF (4th order)	2	OP 07 (Texas Instruments)	Active filter - 60 Hz.
CON	AND gate	1	74LS00 (Philips Semiconductors)	Digital circuit.
	PIC	1	16F877 (Microchip)	Control, A/D converter.

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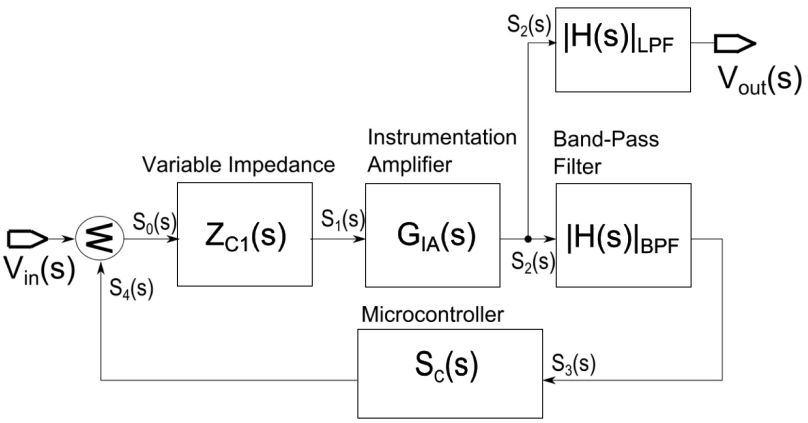

Figure 4. Diagram of the architecture proposed in this paper, providing a global graphical view of the system.

processed, it can lead all other sub-circuits to an uncontrolled state.

Where:

$$S_0(s) = V_{in}(s) - S_4(s) \quad (19)$$

$$S_1(s) = \left(V_{in}(s) - S_4(s)\right) \cdot Z_{C1}(s) \quad (20)$$

$$S_2(s) = G_{IA}(s) \cdot Z_{C1}(s) \cdot \left(V_{in}(s) - S_4(s)\right) \quad (21)$$

$$S_3(s) = G_{IA}(s) \cdot Z_{C1}(s) \cdot |H(s)|_{BPF} \left(V_{in}(s) - S_4(s)\right) \quad (22)$$

$$S_4(s) = \frac{G_{IA}(s) \cdot Z_{C1}(s) \cdot |H(s)|_{BPF} \cdot S_C(s) \cdot V_{in}(s)}{1 + G_{IA}(s) \cdot Z_{C1}(s) \cdot S_C(s) \cdot |H(s)|_{BPF}} \quad (23)$$

$$FT = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_{IA}(s) \cdot Z_{C1}(s) \cdot |H(s)|_{LPF}}{1 + G_{IA}(s) \cdot Z_{C1}(s) \cdot S_C(s) \cdot |H(s)|_{BPF}} \quad (24)$$

Design and Simulation

Design and simulation using description in VHDL_AMS

Initially, the project was described in the VHDL_AMS language and simulated in the Mentor Graphics ADVANCE platform (Mentor Graphics, 2006). For the input stimuli, only the common-mode signal (V_{cm}) was considered, with frequency f_{cm} and Offset = 0. It means that, in the analysis of simulation results (Figure 5), the useful signal (V_{d1} and V_{d2}) will not be present and only the interference (V_{cm}) will be displayed.

The results of two simulations in VHDL_AMS, given a constant Zin_1 and a varying Zin_2, are shown in Figure 5, where three curves are displayed: the first one represents the amplitude control (Control_Step2), in number of resistors (Resistance No); the second one represents the increment or decrement in the resistor bank (Z_{C2}), or the equivalent impedance in ohms, and the third one represents the interference signal (V_{cm}), in volts (V).

In Figure 5, V_{cm} is attenuated and maintained at the lowest level of amplitude possible, by means of the closed loop control which leads to the impedance balancing (Equation 1).

Design and simulation using discrete components

The design and simulations were also performed using the Proteus software "ISIS Professional v7.0" (Labcenter Electronics, 1989-2009). The project was divided as shown in Table 1 in which the electronic components used in the prototype are detailed.

Where:

VAR IMP = variable impedance block;

IA = instrumentation amplifier block;

FIL = filters block;

CON = control block.

Since it wasn't possible to obtain typical digitized pre-stored ECG signals, an equivalent sinusoidal signal was used as a test vector for the simulations, with the same amplitude and frequency characteristics of an ECG signal, besides being strongly influenced by EMI. Figures 6a, b present the simulation results obtained from the circuit designed in the PROTEUS software when characteristic signals obtained from biosensors are applied in order to reduce common-mode noise (V_{cm}).

In Figure 6a, three graphs are shown representing the simulation results of the noise reduction system without feedback or control, upon application of a typical bioelectric signal in the input. The first graph represents the total signal (in the common and differential modes), after amplification by the constant-gain IA ($V_{\_IA\text{-}Out}$), the second graph represents the biosignal at the output of the LPF ($V_{cm} + V_d$), and

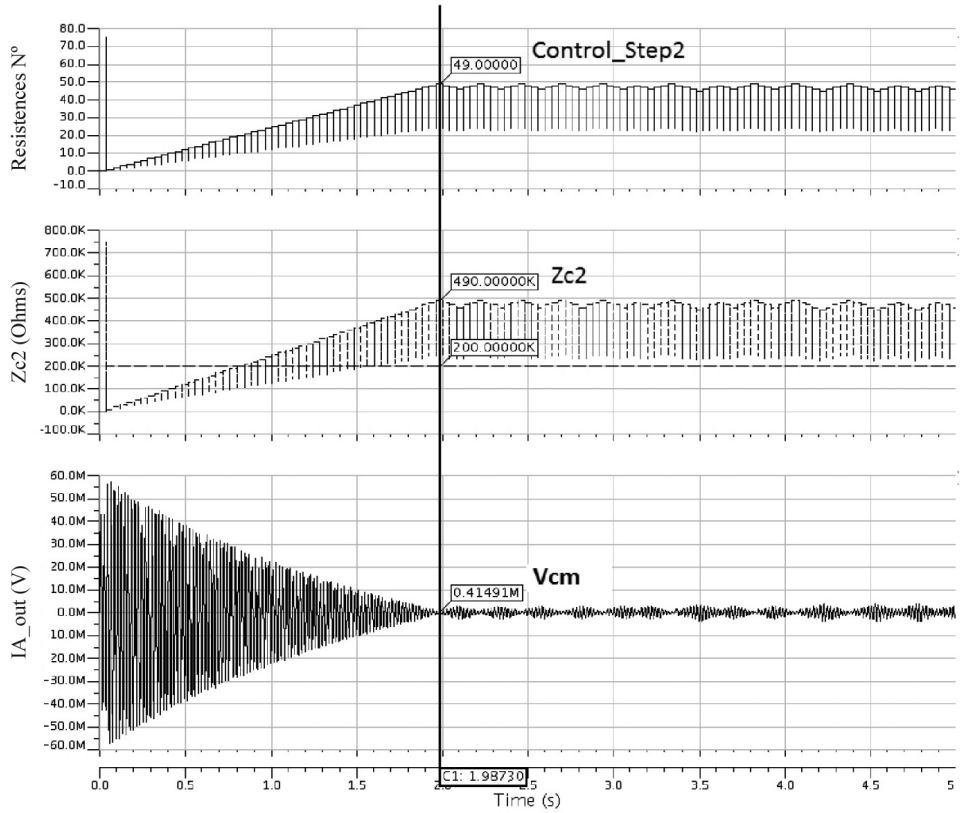

Figure 5. Simulation in VHDL_AMS with feedback control.

the third graph represents the noise at the output of the BPF (V_{cm}). In this case, the system has no feedback and the interference amplitude ranges approximately between a maximum value ($V_{cm\_Max} \approx 1.19$ Vp) and a minimum value ($V_{cm\_Min} \approx 34.0$ mVp). V_d also suffers interference from V_{cm}, such that the useful signal becomes hidden ($V_{cm} >> V_d$). This begins to change as the impedance matching occurs at the IA input, due to the common-mode signal feedback, causing a progressive loss of V_{cm} range, without affecting the V_d amplitude. Thus, the useful signal becomes more visible ($V_{cm} << V_d$).

After feedback is implemented in the circuit, the system simulation yields the graphs in Figure 6b. The top graph represents the output of the IA ($V_{\_IA\text{-}Out}$); the second graph is the output of the LPF filter; and the third graph is the output of the BPF filter.

Results

Prototype circuit

After theoretical analysis and simulation results, a prototype circuit was constructed (Figure 7) where the LPF and BPF filters were implemented in PSOC CY8C27443 microcontrollers.

The prototype tests were performed using as input a signal obtained from ECG electrodes (2223BRQ-3M type, one electrode on each wrist and a third one on the left leg of the patient). Resulting data are shown in Figures 8a, b. In Figure 8a, the circuit has no feedback, i.e., no control. In this case, V_{cm} completely overwhelms the ECG signal (V_d). However, in Figure 8b, the circuit has feedback and the ECG signal is more visible in comparison to the noise. Both Figures 8a, b were obtained inside the electromagnetic noise band (60Hz).

Analyzing the oscillation of the signal in Figure 8b, it is observed that its period is approximately 0.3 seconds, which means a frequency around 3 Hz. Actually, the total oscillation period of the signal shown in the oscilloscope screen (before the signal was highlighted) is approximately 0.018 seconds, which means a frequency around 55.25 Hz. Figure 8b was presented that way only to highlight the achieved results, without modifying or corrupting the obtained data.

Discussion

The main aspects that distinguish this work from Silva's work (Silva, 2003) are the control of the impedance bank and its voltage-divider geometry. In

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this paper, this control is performed both by the up/down counter and the circuit oscillation frequency control. With these adaptations, at first, we notice that the proposed architecture became more efficient for the reduction of V_{cm} noise, both in simulations and in prototype tests. In Silva's work (Silva, 2003), the frequency was kept constant and the counter was used only to vary the resistance bank in a continuous way which did not lead to an effective V_{cm} control, causing the noise to keep oscillating between a maximum and a minimum value. Another aspect is that the control system presented here uses digital data coming from a precise 8-bit A/D converter, and then they are processed by a control algorithm written in the C++ language, running on a microprocessor. This leads to a higher efficacy of the solution proposed in this paper, when compared to the one proposed by Silva. Finally, Silva's work (Silva, 2003) did not produce a physical prototype which could validate his own simulation results. This paper goes beyond simulations and produces a prototype which confirms the results obtained and the modifications proposed.

Analysis of the results obtained shows that the proposed prototype circuit achieved its primary goal, which was reducing the common-mode interference (V_{cm}) while preserving the useful components of the signals to which the system was conceived (V_{d1} and V_{d2}), as shown in Figures 5, 6b and 8b. As for the graph representing V_{cm}, from the analysis of Figure 6, we find that the noise amplitude decreased from 1275 mVpp to 15 mVpp, meaning a percentage attenuation of 98.8%, or –38.59 dB, while the useful signal is preserved.

Figure 5 shows simulation results from the first prototype, which was described using Mentor Graphics' VHDL_AMS platform. This simulation shows the effects of the real-time control of the impedance balancing, from top to bottom: the balancing of the

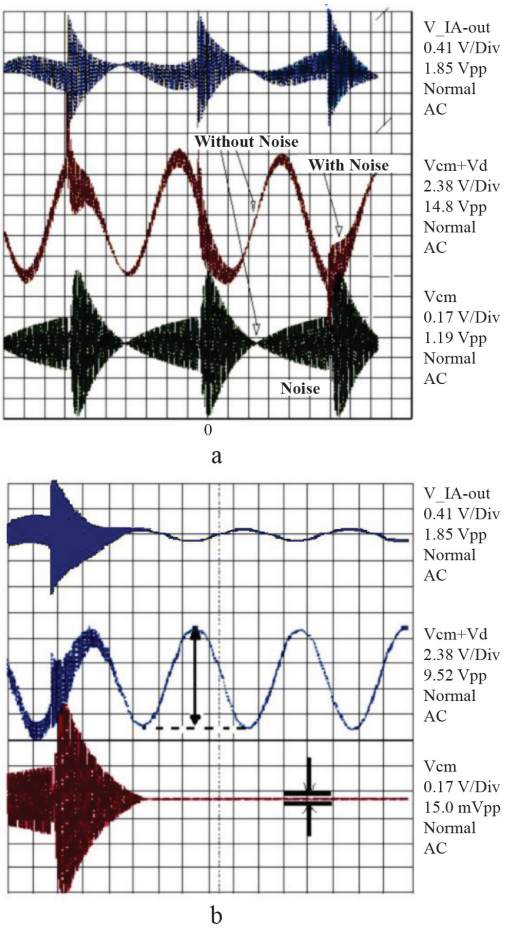

Figure 6. Biosensor: simulation results for the system without feedback (a) and with feedback (b).

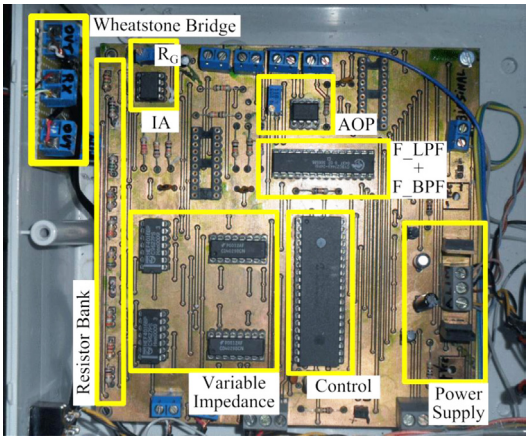

Figure 7. Manufactured prototype in printed circuit board.

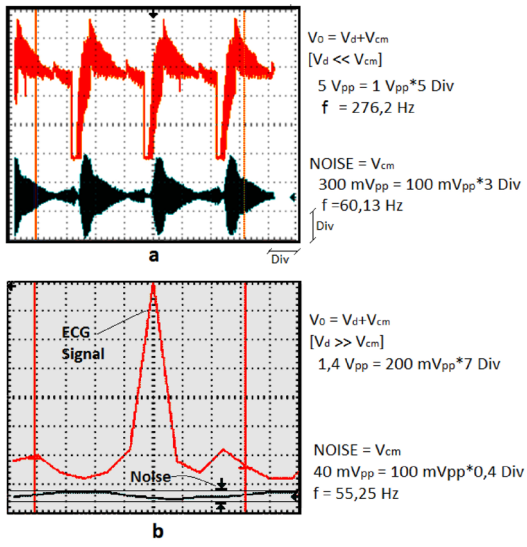

Figure 8. Results obtained with ECG electrodes, (a) circuit without feedback and (b) with feedback.

resistances of the resistor bank "Resistance Nº", the equivalent impedance of one of the IA inputs "Zc_2", and V_{cm} at the IA output "IA_out". The simulated system took around 2 seconds to reach equilibrium, that is, to reduce the input noise, which initially had a 120 mVpp amplitude, to a 0.41 mV value, after feedback was applied to the circuit. This Figure is only concerned with noise analysis. With the present prototype (Figure 7), proper responses were reached in half the time.

Analysis of the results in Figure 8, obtained from the experimental circuit, shows that the results match those obtained from simulation, where a 97.6% reduction was obtained using the sinusoidal signal (or V_{cm} = –32.39 dB), and a 86.66% reduction was achieved using ECG electrodes (or V_{cm} = –17.50 dB), Figures 8a, b.

This paper addressed the reduction of common-mode noise, specially the one originating from electromagnetic sources. We introduced the impedance balancing concept and proposed a modified architecture for V_{cm} noise reduction, using dynamic input impedance balancing (Z_{VAR}). A circuit was designed and simulated in VHDL_AMS, and also designed and simulated in discrete circuit form, employing close-to-real parameter values of discrete components found in the market, and at the end, a prototype circuit was built and tested.

Excellent results were obtained, validating the proposed architecture and its application to signals that need to be controlled without the use of complex circuits or filters, many of which will override both the noise signals (in common-mode), but also the components of the useful signal (in differential mode).

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Authors

João Francisco Ribeiro Negrão*
Instituto de Tecnologia – ITEC, Universidade Federal do Pará – UFPA, Rua Augusto Corrêa, 01, Guamá, CEP 66075-110, CP 479, Belém, PA, Brasil.

Guilherme Augusto Limeira Araujo, Carlos Tavares da Costa Júnior, Daniel Cardoso de Souza
Faculdade de Engenharia Elétrica, Universidade Federal do Pará – UFPA, Belém, PA, Brasil.